UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/802,566	03/17/2004	Mou-Shiung Lin	085027-0109	3507

89518 7590 05/16/2012

McDermott Will & Emery LLP
600 13th Street, NW
Washington, DC 20005-3096

EXAMINER	
ARORA, AJAY	
ART UNIT	PAPER NUMBER
2892	

NOTIFICATION DATE	DELIVERY MODE
05/16/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mweipdocket@mwe.com
SIP_Docket@mwe.com
ocpat_uspto@qualcomm.com

Office Action Summary	Application No.	Applicant(s)	
	10/802,566	LIN, MOU-SHIUNG	
	Examiner	Art Unit	
	AJAY K. ARORA	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2012*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1,7,9-12,15,17-19,21,22,25,27,91,96-99,101-103,108-114 and 116-139* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 1,7,9-12,15,17-19,21,22,25,27,91,96-99,101-103,108-114 and 116-139.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 7, 9-12, 15, 17-19, 21-22, 25, 27, 91, 96-99, 101-103, 108-114, and 116-139 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US 6,303,423) of prior record, hereinafter Lin, in view of Nakanishi (US 6,921,980) of prior record, hereinafter Nakanishi.

Regarding claim 1, Lin (refer to Figures 1-2 and 10) teaches a circuit chip comprising:

a semiconductor substrate (10);

a transistor in and on said semiconductor substrate (Col. 7, lines 27-30);

multiple metal and dielectric (14, also see Col. 7, lines 36-39) layers over said semiconductor substrate;

a first contact pad (16 shown on left side of Figure 10) over said semiconductor substrate;

a second contact pad (16 shown on right side of Figure 10) over said semiconductor substrate;

a passivation layer (18) over said multiple metal and dielectric layers (14), wherein said passivation layer comprises a nitride (Col. 8, lines 52-56), wherein a first opening in said passivation layer (18) is over a first contact point of said first contact pad (16 shown on left side of Figures 1-2 and 10) and said first contact point is at a bottom of said first opening (i.e. on bottom surface of first contact pad 16), and wherein a second opening in said passivation layer (18) is over a second contact point of said second contact pad (16 shown on right side of Figure 10) and said second contact point is at a bottom (i.e. bottom of opening in passivation layer 18, where the bottom of opening touches the top of second contact pad) of said second opening;

a power metal structure (structure directly above 16 shown on the right side, see Col. 8, lines 21-24) over said passivation layer (18) and on said first contact point, wherein said power metal structure is connected to said first contact point through said first opening (as first contact point is in the first opening and power metal structure is over the first opening), wherein said power metal structure comprises a metal layer;

a ground metal structure (structure directly above 16 shown on the left side, see Col. 8, lines 21-24) over said passivation layer (18) and on said second contact point, wherein said ground metal structure is connected to said second contact point through said second opening (as second contact point is in the second opening and ground metal structure is over the second opening), wherein said ground metal structure comprises a metal layer;

a capacitor (54) over said passivation layer (18), vertically over said power and ground metal structures (i.e. metal structures directly above 16 shown on the right side and left side respectively, see Col. 8, lines 21-24), and vertically over said first contact point (as first contact point is part of first contact pad 16 shown on left side of Figures 1-2, as explained above; and it can be seen in Figure 10 that at least a part of the capacitor 54 is vertically over 16)

a first solder joint (joint corresponding to one of the 52) vertically over said first contact point (as explained above, noting that at least part of 52 is vertically over 16, as seen in Figure 10) and between a first terminal of said capacitor (first terminal of capacitor 54 that is just above first solder contact and which bonds with the first solder contact forming an electrical connection to the corresponding capacitor for input/output) and said power metal structure, wherein said first solder joint connects said first terminal to said power metal structure; and

a second solder joint (solder joint corresponding to the other of the 52) between a second terminal of said capacitor (second terminal of capacitor 54 that is just above second solder contact and which bonds with the second solder contact forming an electrical connection to the capacitor for input/output) and said ground metal structure, wherein said second solder joint connects said second terminal to said ground metal structure.

Lin does not teach that the metal layer of said power metal structure and said ground metal structure is a “copper layer”; that “said power structure has a first region not vertically over said first opening"; and said power (and ground) metal structures

each has a region (first region and second region, respectively) used to be wirebonded thereto for connection made to a level of packaging. Nakanishi (refer to Figures 2a-2e and 3) teaches an integrated circuit with a semiconductor substrate (2) and a capacitor (8) mounted to a metallization structure comprising a copper layer (Col. 4, lines 58-63), which can server as a power or ground structure, wherein the metallization structure has a region (region over 3 that is on the right side of Figures 2a and 2e that is connected to terminals of 8 - see Figure 2e - and also to wirebond 12 - see Figure 3) used to be wirebonded (by wirebonds 12) thereto for connection to next level of packaging (15). Nakanishi also teaches that the above said region (of the metallization structure used to be wirebonded) may be offset with respect to a first and second contact points of respective first and second contact pads (contact pads corresponding to 7 of Figure 2d) to which a respective first and second terminal of a capacitor (8) are mounted (see Figure 2e), such that the first terminal (shown on right in Figure 2d and 2e) is vertically over said first contact point (best seen in Figures 2c and 2d). The above said offset enables not only to connect the capacitor (8) to the metallization structure but also provides space (by above set offset) for wirebonding to the next level of packaging. In view of the above, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify Lin in view of Nakanishi so that the metal layer of said power metal structure and said ground metal structure is a “copper layer”; that “said power structure has a first region not vertically over said first opening"; and said power (and ground) metal structures each has a region (first region and second region, respectively) used to be wirebonded thereto for connection made to a

level of packaging. The ordinary artisan would have been motivated to modify Lin for at least the purpose of providing routing for interconnects to contact pads that are closer to the periphery of the semiconductor substrate (compared to the capacitor, thus allowing flexibility of placing the capacitor in a central location on the semiconductor substrate, as shown in Figure 3b of Nakanishi), while still being able to connect to the ground or power of next level of packaging without excessive wirebond length and a high electrical conductivity metal, like copper, which improves electrical performance and which allows long interconnect length, to connect to next level of packaging.

Regarding claim 7, Lin teaches substantially the claimed structure but does not teach that said ground metal structure further comprises “a gold layer" over said copper layer of said ground metal structure. Nakanishi teaches that copper metallization, which is usable as a ground metal structure, may further comprise a gold layer over said copper layer (Col, 4, lines 58-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin so that said ground metal structure further comprises a gold layer over said copper layer of said ground metal structure. The ordinary artisan would be motivated to modify Lin at least for the purpose of providing a layer that has increased resistance to corrosion.

Regarding claim 91, Lin teaches that said passivation layer (18) may comprise silicon nitride (Col. 7, lines 49-53).

Regarding claim 96, Lin teaches that said ground metal structure further comprises a nickel layer over said copper layer (Col. 9, lines 26-30) of said ground metal structure.

Regarding claim 97, Lin (refer to Figures 1-2 and 10) as modified in view of Nakanishi for claim 1, teaches a polymer layer (20 of Figure 10 of Lin) on said power and ground metal structures (as explained in rejection of claim 1), wherein a third opening (opening in 20 directly over 16 shown on right) in said polymer layer (20) is over a third contact point (point just above 16) of said power metal structure , and said third contact point is at a bottom of said third opening (as the point is just above 16), wherein a fourth opening in said polymer layer (opening in 20 directly over 16 shown on left) is over a fourth contact point of said ground metal structure, and said fourth contact point is at a bottom of said fourth opening (as the point is just above 16), wherein said first solder joint (solder joint corresponding to one of 52) is between said first terminal (first terminal of capacitor 54, as explained in rejection of claim 1) and said third contact point and connects said first terminal to said third contact point through said third opening (opening in 20 closest to 52), and said second solder joint (solder joint corresponding to other of 52) is between said second terminal (second terminal of capacitor 54, as explained in rejection of claim 1) and said fourth contact point, and connects said capacitor to said fourth contact point through said fourth opening (opening in 20 closest to 52).

Regarding claims 113 and 114, Lin (refer to Figures 1-2 and 10) teaches that said polymer layer (20) comprises polyimide, wherein said polymer layer has a thickness between 2 and 150 micrometers (Col. 8, lines 66-67 and Col. 7, lines 1-3).

Regarding claim 116, Lin teaches that said passivation layer (18) may further comprise an oxide (Col. 8, lines 54-56).

Regarding claim 117, Lin teaches substantially the claimed structure including that passivation layer comprises an oxide but does not teach that the passivation layer comprises silicon oxide. Nakanishi teaches that a passivation layer may comprise silicon oxide (Col. 4, lines 19-23). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Lin so that the passivation layer comprises silicon oxide. The ordinary artisan would have been motivated to modify Lin for at least the purpose of forming a passivation layer that has excellent moisture resistance and which is closely matched in coefficient of thermal expansion with silicon substrates.

Regarding claim 123, Lin (refer to Figures 1-2 and 10) as modified in view of Nakanishi for claim 1, teaches a polymer layer (20 of Figure 10 of Lin) on said power and ground metal structures (as explained in rejection of claim 1), wherein a third opening (opening in 20 directly over 16 shown on right) in said polymer layer (20) is over said first region, and said first region is at a bottom of said third opening (in polymer layer 20), and wherein a fourth opening (opening in 20 directly over 16 shown on left) in said polymer

layer is over said second region, and said second region is at a bottom of said fourth opening.

The limitations of claims 124 and 125 have already been addressed in claims 113 and 114.

Regarding claim 126, Lin (refer to Figures 1-2 and 10) as modified in view of Nakanishi for claim 1, teaches a polymer layer (20 of Figure 10 of Lin) on said power and ground metal structures (as explained in rejection of claim 1), wherein a third opening (opening in 20 directly over 16 shown on right) in said polymer layer (20) is over a third contact point (point just above 16) of said power metal structure , and said third contact point is at a bottom of said third opening (as the point is just above 16), wherein a fourth opening in said polymer layer (opening in 20 directly over 16 shown on left) is over a fourth contact point of said ground metal structure, and said fourth contact point is at a bottom of said fourth opening (as the point is just above 16) wherein a fifth opening in said polymer layer (upper opening of 20 directly above third opening) is over said first region, and said first region is at a bottom of said fifth opening, and wherein a sixth opening in said polymer layer (upper opening of 20 directly above fourth opening) is over said second region, and said second region is at a bottom of said sixth opening, wherein said first solder joint (solder joint corresponding to one of 52) is between said first terminal (first terminal of capacitor 54, as explained in rejection of claim 1) and said third contact point and connects said first terminal to said third contact point through

said third opening (opening in 20 closest to 52), and said second solder joint (solder joint corresponding to other of 52) is between said second terminal (second terminal of capacitor 54, as explained in rejection of claim 1) and said fourth contact point, and connects said capacitor to said fourth contact point through said fourth opening (opening in 20 closest to 52).

The limitations of claims 127 and 128 have already been addressed in claims 113 and 114.

Regarding claim 9, Lin (refer to Figures 1-2 and 10) teaches an integrated circuit chip, comprising:

a semiconductor substrate (10);

a transistor in and on said semiconductor substrate (Col. 7, lines 27-30);

multiple metal and dielectric (14, also see Col. 7, lines 36-39) layers over said semiconductor substrate;

a first contact pad (16 shown on left side of Figure 10) over said semiconductor substrate;

a passivation layer (18) over said multiple metal and dielectric layers (14), wherein a first opening in said passivation layer (18) is over a first contact point of said first contact pad (16 shown on left side of Figure 10) and said first contact point is at a bottom of said first opening (i.e. on bottom surface of first contact pad 16), wherein said passivation layer comprises a nitride (Col. 8, lines 52-56);

a second contact pad (16 shown on right side of Figure 10) over said semiconductor substrate

a capacitor (54, also see Col. 14, lines 21-24) over said passivation layer (18);

said capacitor (54) comprising a terminal (terminal of capacitor 54 that is directly over 16 shown on left side of Figure 10), that is electrically coupled to and vertically over (best seen in Figure 10) said first contact point (16 shown on left side of Figure 10).

Lin also does not teach that the second contact pad is “not vertically over said first opening, said second contact pad connected to said first contact point through said first opening”, and that “said second contact pad comprises a first gold layer with a thickness greater than 1 micrometer”. Except for the last limitation related to thickness of gold, these limitations are similar to those already addressed in claim 1 because the limitation of “the second contact pad" of claim 9 that is “not vertically over said first opening, said second contact pad connected to said first contact point through said first opening” reads on the limitation of claim 1 that recites “said power metal structure has a first region not vertically over said first opening configured to be wirebonded thereto for connection made to a next level of packaging” (see lines 14-16 of claim 1) – with the provided motivation for claim 1 also providing motivation for the “second contact” of claim 9 being "not vertically over said first opening...". The limitation of "said second contact pad comprises a first gold layer" is similar to that already addressed for claim 17. As for the thickness of first gold layer being "greater than 1 micrometer", the specific thickness of the gold layer is considered to involve routine optimization, which

has been held to be within the level of ordinary skill in the art. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Lin such that said second contact pad comprises a gold layer with a thickness greater than 1 micrometer and there is an additional metal layer between said solder connection and said second contact pad. The ordinary artisan would be motivated to modify Lin at least for the purpose of providing a gold layer that has optimal thickness for its intended purpose (such as providing resistance against corrosion, increasing wettability, etc.) for the given design and providing the additional metal layer to provide a barrier layer between the solder and the underlying device.

Regarding claims 10-11, the limitation of “a fourth contact pad over said semiconductor substrate” is similar to the “second contact pad” already addressed in view of Nakanishi (note that Figure 3b of Nakanishi shows multiple wirebonded pads and they read on a second and third contact pad). The additional limitation that the third contact is used for wirebonding for “connection made to next level of packaging” has also earlier been addressed in view of Nakanishi. The limitation that “said second contact point is at a bottom of said second opening” is also similar to that addressed before.

Regarding claim 12, Lin (refer to Figures 1-2 and 10) as modified in view of Nakanishi teachs a fourth contact pad (16 in Figure 10 of Lin) over said semiconductor substrate (10), wherein a second opening in said passivation layer (18) is over a second contact

point of said fourth contact pad (16), and said second contact point is at a bottom of said second opening. The claimed “fifth contact pad” on said second contact point is similar to the wirebonded pad of Nakanishi (as Nakanishi has multiple wirebonded pads, as described for claim 15; i.e. said fourth contact pad is used to be wirebonded thereto for connection made to next level of packaging.

Regarding claim 118, the limitation of a contact pad or metallization comprising a gold layer has already been addressed in claims 9 and 17. It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Lin so that so that said fourth contact pad comprises a second gold layer. The ordinary artisan would have been motivated to modify Lin for at least the purpose of providing a second layer of high conductivity and corrosion resistance material to further improve corrosion resistance.

Regarding claim 98, the said capacitor (54) of Lin is capable of functioning a decoupling capacitor.

The limitations of claim 99 have already been addressed in claim 91.

Regarding claim 119, Lin (refer to Figures 1-2 and 10) as modified in view of Nakanishi for claim 1, teaches a polymer layer (20 of Figure 10 of Lin) over said passivation layer (18), wherein a second opening (opening in 20 directly over 16 shown on right) in said polymer layer (20) is over a second contact point (point just above 16) of said second

contact pad (16 shown on right side of Figure 10), and said second contact point is at a bottom of said second opening (as the point is just above 16), and wherein said solder joint (corresponding to 50) is between said terminal (terminal of capacitor 54) and said second contact point (point just above 16) and connects said terminal to said second contact point through said second opening, wherein said third contact pad (pad corresponding to 50 of Figure 10) is between said solder joint and said second contact point.

The limitations of claim 120 have already been addressed in claims 113 and 114.

The limitations of claims 121 and 122 have already been addressed in claims 116 and 117.

Regarding claim 15, Lin (refer to Figures 1-2 and 10) teaches an integrated circuit chip, comprising:

a semiconductor substrate (10);

a transistor in and on said semiconductor substrate (Col. 7, lines 27-30);

multiple metal and dielectric (14, also see Col. 7, lines 36-39) layers over said semiconductor substrate;

a first contact pad (16 shown on left side of Figure 10) over said semiconductor substrate;

a passivation layer (18) over said multiple metal and dielectric layers (14), wherein said passivation layer comprises a nitride (Col. 8, lines 52-56), and wherein a first opening in said passivation layer (18) is over a first contact point of said first contact pad (16 shown on left side of Figure 10) and said first contact point is at a bottom of said first opening (i.e. on bottom surface of first contact pad 16);

a second contact pad (contact pad directly over first contact pad 16 which connects first contact pad to 50) over said semiconductor substrate, wherein said second contact pad is connected to and vertically over (best seen in Figure 10) said first contact point (contact point of said first contact pad 16 shown on left side of Figure 10) through said first opening (in passivation layer 18);

a first polymer layer (20) over said passivation layer (18), wherein a second opening (opening in 20 through which 16 connects to 50) in said first polymer layer (20) is over a second contact point (contact point at surface of second contact pad that is nearest to 16) of said second contact pad, and said second contact point is at a bottom of said second opening;

a capacitor (54, also see Col. 14, lines 21-24) over said first polymer layer (20), said capacitor having a terminal that is vertically over said second contact point; and

a solder joint (joint corresponding to 52, also see Col. 14, lines 16-21) between said second contact point and a terminal of said capacitor (54), wherein said solder joint connects said terminal to said second contact point.

Lin does not teach the claimed “third contact pad” for wirebonding and its location, that it “is not vertically over said first contact point”. Nakanishi (refer to Figures 2a-2e and 3) teaches an integrated circuit with a semiconductor substrate (2) and a capacitor (8) mounted to a first and second contact pad (contact pads to nearest to 8 to which 8 is connected), and a third contact pad (3 to which wirebond 12 is connected in Figure 3) over said semiconductor substrate (2), wherein said third contact pad is connected to first and second contact pads through an opening in the passivation layer (Col. 4, lines 19-23), wherein the position of said third contact pad (3) is not vertically over said first contact point (on first contact pad) and wherein said third contact pad has a region used to be wirebonded (to wirebond 12 of Figure 3b) thereto for connection made to a next level of packaging (15 of Figure 3b). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Lin in view of Nakanishi as above to include the missing limitations such as the claimed third contact pad for wirebonding and its location, such as the position of said third contact pad is not vertically over said first contact point. The ordinary artisan would have been motivated to modify Lin for at least the purpose of providing a third contact pad that is closer to the periphery of the semiconductor substrate compared to the capacitor (which allows flexibility of placing the capacitor in a central location on the semiconductor substrate, as shown in Figure 3b of Nakanishi), while still being able to connect to the next level of packaging without excessive wirebond length.

Regarding claim 17, Lin teaches substantially the claimed structure but does not teach that said second contact comprises a “gold” layer. However, the use of a gold layer, such as a gold plating, over a contact metallization layer is well known in the art (see Nakanishi, Col, 4, lines 58-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Lin so that said second contact comprises a gold layer. The ordinary artisan would be motivated to modify Lin at least for the purpose of providing a layer that has excellent conductivity and resistance to corrosion.

Regarding claim 18, Lin teaches substantially the claimed structure but does not teach that said second contact comprises a “copper” layer. However, the use of copper for contact metallization is well known in the art (see Nakanishi, Col. 4, lines 58-63). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Lin so that said second contact comprises a copper layer. The ordinary artisan would be motivated to modify Lin at least for the purpose of using a high thermal and electrical conductivity metal for the second contact to minimize electrical losses and improved functionality.

Regarding claims 19 and 21, Lin as modified above in view of Nakanishi for claim 15, teaches a ground metal structure or a power metal structure (Col. 8, lines 21-23) connected to said capacitor (54 of Figure 10 of Line), to said wirebond (12 of Figure 3b of Nakanishi) and to said first contact pad (first contact pad 16 of Figure 10 of Lin).

Regarding claim 22, Lin (refer to Figures 1-2 and 10) teaches that said second contact point (as explained in rejection of claim 15) is further vertically over said passivation layer (18).

Regarding claim 25, Lin (refer to Figures 1-2 and 10) teaches that said passivation layer (18) may comprise silicon nitride (Col. 7, lines 49-53).

Regarding claim 27, Lin teaches substantially the claimed structure but does not teach that said third contact comprises “gold”. The use of gold for a contact and its corresponding motivation has already been addressed in claim 7.

Regarding claim 101, the capacitor (54) of Lin (refer to Figures 1-2 and 10) is capable of functioning as a decoupling capacitor.

Regarding claim 102, Lin (refer to Figures 1-2 and 10), as modified in view of Nakanishi for claim 15, teaches a third opening in said first polymer layer is over said region of said third contact pad , and said region is at a bottom of said third opening. Note that an opening in the first polymer layer is a necessary condition for wirebonding taught by Nakanishi.

Regarding claim 103, Lin (refer to Figures 1-2 and 10) teaches that the said first polymer layer (20) comprise polyimide (Col. 9, lines 4-5).

The limitations of claim 108 have already been addressed in claim 125.

Regarding claims 109 and 110, said first, second and third contact pads are configured to be capable of receiving ground voltage or power supply voltage (Col. 8, lines 21-24).

The limitations of claims 111 and 112 have already been addressed in claims 116 and 117.

Regarding claim 129, Lin (refer to Figures 1-2 and 10) teaches an integrated circuit chip, comprising:

a semiconductor substrate (10);

a transistor in and on said semiconductor substrate (Col. 7, lines 27-30);

multiple metal and dielectric (14, also see Col. 7, lines 36-39) layers over said semiconductor substrate;

a first contact pad (16 shown on left side of Figure 10) over said semiconductor substrate;

a passivation layer (18) over said multiple metal and dielectric layers (14), wherein a first opening in said passivation layer (18) is over a first contact point of said first contact pad (16 shown on left side of Figure 10) and said first contact point is at a

bottom of said first opening (i.e. on bottom surface of first contact pad 16), wherein said passivation layer comprises a nitride (Col. 8, lines 52-56);

a capacitor (54, also see Col. 14, lines 21-24) over said passivation layer (18), said capacitor comprising a terminal (terminal of 54 corresponding to 52 shown on left side of Figure 10) that is vertically over said first contact point (contact point corresponding to first contact pad 16 shown on left side of Figure 10);

a solder joint (solder joint corresponding to 52 shown on left side of Figure 10, also see Col. 14, lines 16-21) between said terminal (i.e. terminal of 54 corresponding to 52 shown on left side of Figure 10) of said capacitor (54);

a third contact pad (pad corresponding to 50 of Figure 10 to which 52 is soldered).

Lin does not teach “a second contact pad over said semiconductor substrate, wherein said second contact pad is connected to but not vertically over said first contact point through said first opening”. As such, Lin also does not teach other details related to "said second contact pad" such as the capacitor is "over" said second contact pad; that said solder joint is "between said terminal of said capacitor and said second contact pad, wherein said solder joint connects said terminal to said second contact pad”; that the third contact pad is “between said solder joint and said second pad”; and that “a contact area between said third contact pad and said second contact pad is not vertically over said first contact point”. However, the required "second contact pad" is similar to the limitation of claim 1 that requires "a region used to be wirebonded thereto for connection to next level of packaging”, which is essentially a

contact pad that is offset from (i.e. not vertically over) the pad which is vertically under a capacitor terminal to facilitate wirebonding (as explained for claim 1 in view of Nakanishi). Modifying Lin in view of teachings of Nakanishi to include an additional pad for wirebonding described above leads to a structure where the additional pad for wirebonding is “a second contact pad” such that the second contact pad over said semiconductor substrate, wherein said second contact pad is connected to but not vertically over said first contact point through said first opening (due to the offset described above); that the capacitor is "over" said second contact pad (as second contact pad is at the same level as first contact pad – see Nakanishi Figures 2e and 3); that said solder joint is "between said terminal of said capacitor and said second contact pad (as it electrically connects them), wherein said solder joint connects (i.e. electrically connects as described above) said terminal to said second contact pad ; that the third contact pad (contact pad of 50) is between said solder joint (52) and said second pad (as 50 extends to and electrically connects to said second pad used for wirebonding); and that a contact area (i.e. area corresponding to metallization that extends between said third contact pad and said second contact pad – see Figure 2e and 3 of Nakanishi) between said third contact pad and said second contact pad is not vertically over (because said third contact pad is not vertically over) said first contact point. Thus the same obviousness criteria and corresponding motivation as applied to claim 1 in view of Nakanishi also applies here.

The limitation of "said second contact pad comprises a first gold layer" is similar to that already addressed for claim 17. As for the thickness of first gold layer being

"greater than 1 micrometer", it has already been addressed for claim 9. The limitation "said third contact pad is finished with a solder wettable material comprising gold" is similar to claims 17-18.

Regarding claims 130 and 131, the "fourth contact pad" is the other wirebonded pad of Nakanishi which is also "used to be wirebonded thereto for connection to next level of packaging". It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Lin so that Lin includes the claimed "fourth contact pad over said semiconductor substrate" as claimed. The ordinary artisan would have been motivated to modify Lin for at least the purpose of providing a fourth pad near the periphery of the substrate which would provide a wirebond connection to the next level of packaging (15 of Nakanishi) without unduly long wirebonds (so that electrical performance is not degraded).

Claim 132 requires "fourth contact pad" and "fifth contact pad" which have a similar function of facilitating interconnection and providing wirebonding to next level of packaging as discussed above. It would have been obvious to one of ordinary skill in the art to use additional contact pads teaching of Nakanishi in Lin to create a structure, as claimed, because such structure is considered to be a duplication of parts that has no patentable significance unless a new unexpected result is produced. In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960), MPEP 2144.04.

Claim 133 is similar to claim 118 and hence the same reasoning applies.

Claim 134 is similar to claim 98 and hence the same reasoning applies.

Claim 135 is similar to claim 25 and hence the same reasoning applies.

The limitations of claim 136 have already been addressed in claim 119.

The limitations of claim 137 have already been addressed in claim 125.

The limitations of claims 138 and 139 have already been addressed in claim117.

Response to Arguments

3. Applicant's arguments with respect to claim 129 and its dependent claims have been considered but are moot because the arguments do not apply to any of the references being used in the current rejection. Although the same is also true for base claims 1, 9 and 15, some of the arguments are still relevant because the references used are same as before but with some differences due to amendments. These relevant arguments will be addressed here.

4. On page 13, last paragraph to page 19, 2nd paragraph, applicant argues about rejection of claim 1. More specifically, applicant argues that "applying the teachings of Nakanishi to the chip of Lin would connect the bond wire to the contact plug 50 that is vertically over the contact pad 16 and would then offset the discrete component 54 form the contact plug 50" (see page 17, last paragraph). This argument is not persuasive. Referring to Figures 2 and 3 of Nakanishi, it suggests keeping the discrete component (54 of Figure 10 of Lin or its equivalent 8 of Figure 2e and 3 of Nakanishi) as is, but

extending a part of the metallization towards a periphery of the device so as to provide an additional pad that is electrically connected to the passive component but being closer to periphery of the device, is suitable for wire bonding. In implementing this, there is no need to "offset the discrete component 54" (as argued by the applicant). Applicant also argues that Nakanishi forms "isolated wiring traces 5 of copper" (see page 18, 2nd paragraph, especially last sentence). It appears that applicant is alleging that wiring traces 5 of Nakanishi are not capable of interconnecting components or component pads. This argument is not persuasive as it is well known in the art that the very function of traces in this context is to achieve interconnection. Even if a trace is not connected to other traces, it can still interconnect two components when the respective components are connected, for example, one at each end of the trace, thus enabling interconnection of components.

5. On page 18, last paragraph, applicant argues that "Nakanishi is silent as to any further metal layers over the traces 5". However, Nakanishi is not being used to teach "further metal layers" (that feature is taught by Lin). In response to applicant's above arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

6. On page 18, last paragraph, applicant argues that “Wires 12 can be bonded only to the pads 3 from which the sputtered TiW and Cu were removed”. This argument is not clear. Applicant's claim only recites "configured to be wirebonded thereto for connection made to said next level of packaging" and this has been addressed in view of Nakanishi which also teaches wirebonds and as such teaches regions that are configured to be wirebonded thereto for connection made to said next level of packaging – if this was not the case, wirebonding shown in Nakanishi would not be possible.

7. Arguments presented for claim 9 (pages 19-20), claim 15 (page 20-21) and claim 129 (page 22-23) are also similar (also see revised rejection of claim 129 in view of amendments).

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AJAY K. ARORA whose telephone number is (571)272-8347. The examiner can normally be reached on Mon through Fri, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/AJAY K. ARORA/

Primary Examiner, Art Unit 2892